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Procedure for Characterizing Time- Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics

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PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

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PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

Foreword

This document is intended for use MOS integrated circuit manufacturing. It describes a test procedure for estimating the acceleration parameters of “wear-out” or Time-Dependent-Dielectric Breakdown (TDDB) of ultra-thin ($t_{ox} < 5$ nm) gate oxides. This document also describes robust techniques to detect breakdown and analysis methods for ultra-thin dielectric films that exhibit large tunneling currents and soft breakdown. It includes one informative annex on supplemental data analysis.

The purpose of this document is to describe test procedures for characterizing the reliability of ultra-thin gate oxides. It does not specify acceptance or rejection criteria for any of the described procedures.

The material contained within this standard is formulated under the cognizance of JEDEC 14.2 Committee and approved by the JEDEC Board of Directors.

PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS

(From the JEDEC Board ballot JCB-03-16, formulated under the cognizance of the JC-14.2 Committee on Wafer Level Reliability)

1 Scope

This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or “wear-out” of thin gate dielectrics. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. Unlike highly accelerated ramp tests that are designed to be extremely fast and performed at the wafer-level, the constant voltage test procedure may be conducted over long periods of time. It may be applied at the wafer-level or with packaged devices.

For ultra-thin films breakdown can be difficult to detect. Ultra-thin films exhibit large tunneling currents and soft or noisy breakdown characteristics; special techniques must be used to detect breakdown under these circumstances.

This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

2 Overview

This document describes a constant voltage stress (CVS) test used to obtain acceleration parameters required to predict Time-Dependent Dielectric Breakdown (TDDB) of ultra-thin gate dielectrics used in advanced CMOS microelectronics.

It has been observed that breakdown in ultra-thin SiO₂ films ($t_{ox} < 5$ nm) becomes “soft” or noisy. At the breakdown event abrupt changes in current may not occur and device breakdown is difficult to detect. This document describes special methods for soft breakdown detection.

The complete CVS test procedure includes four sub-tests. First, a pre-characterization test is performed to determine operating points required by the CVS test. Second, a pre-CVS test is performed to remove damaged capacitors prior to starting the CVS test. Third, the CVS test is conducted, and finally, a post-CVS test is performed to confirm that a valid failure has occurred during the CVS test.

Several parameters are recorded as a result of the test including time-to-breakdown (t_{bd}), charge-to-breakdown (Q_{bd}) and the accumulation of stress-induced leakage current (SILC).

3 Terms and definitions

The following symbols are used in this document. They have been listed alphabetically for the convenience of the reader.

A_{oxide} (cm²) Oxide gate area.

E_{ox} (V/cm) E_{ox} is the oxide electric field. The general formula for E is:

$$E_{ox} = V_{ox} / t_{ox}, \quad (1)$$

where V_{ox} is the oxide voltage and t_{ox} is the oxide thickness. t_{ox} must be determined by a consistent, documented method. It is important to point out that the applied voltage is not necessarily the voltage across the oxide. Ultra-thin oxides exhibit quantum confinement effects and gate electrode depletion effects effectively reducing the voltage across the oxide. The method of determining t_{ox} or a reference to the documented standard must be included in the data report.

E_{bd} (V/cm) The estimated oxide electric field just before oxide breakdown. (see Annex).

I_{bd} (A) Oxide current measured just before oxide breakdown.

I_{comp} (A) The maximum current of the voltage-forcing equipment. Often the user can specify a compliance limit for a particular test.

I_{leak} (A) An optional pre-test leakage current at which the device is considered a yield failure.

I_{meas} (A) The measured oxide current.

I_{SILC} (A) The stress-induced leakage current measured at V_{SILC}. This value is measured and compared during the constant voltage test if the stress interruption method is used to detect breakdown.

I_{use} (A) The typical measured current through the oxide at the normal use voltage.

I_{stress} (A) The oxide current measured during the CVS test.

I_{previous} (A) The previously measured oxide current.

3 Terms and definitions (cont'd)

J (A/cm²) The oxide current density calculated by dividing the oxide current by the oxide area (A_{oxide}).

Q_{bd} (coulombs) The accumulated charge in coulombs that passed through the oxide prior to breakdown. Q_{bd} is defined as:

$$Q_{bd} = \int_{t=0}^{t=t_{bd}} I(t)dt \quad (2)$$

where t is time. The Q_{bd} is calculated as the integral from t = 0 to t = t_{bd} where t_{bd} is the time of the last measurement just prior to breakdown.

q_{bd} (C/cm²) The accumulated charge density is calculated as:

$$q_{bd} = \frac{Q_{bd}}{A_{oxide}} \quad (3)$$

t_{bd} (s) The recorded time at oxide failure.

t_{int} (s) The time that stress is applied before the stress is interrupted and I_{SILC} is measured during the stress interruption technique for detecting breakdown.

t_{meas} (s) The time interval for measuring the stress current (I_{stress}) during the constant voltage test.

t_{ox} (nm) Physical thickness of gate oxide.

t_{record} (s) The time interval for recording current measurements (I_{meas}) during the constant voltage test.

t_{wait} (s) The wait time after stress is interrupted before I_{SILC} is measured during the stress interruption technique for detecting breakdown.

V_{SILC} (V) The voltage at which the stress-induced leakage current (I_{SILC}) is measured.

V_{stress} (V) The oxide stress voltage.

V_{use} (V) The test voltage that is applied during pre- and post-test to determine device validity. This voltage is usually the power supply voltage or use voltage of the technology.

4 Constant voltage test procedure

4.1 Test configuration

The CVS test may be performed either in inversion or in accumulation. The capacitor test structure must be carefully selected depending on your product requirements.

For ultra-thin oxides (with $t_{ox} < 5$ nm), there is evidence that the driving force for dielectric breakdown is the gate voltage (voltage difference between the Fermi level positions in the anode and cathode) and not the oxide voltage (voltage difference between the top of the conduction bands in the anode and cathode). It is therefore important to minimize any voltage drops in the substrate and gate wiring due to series resistance that may lead to errors in the actual applied gate voltage.

For inversion testing the test capacitor must be bounded by a diffusion layer that provides the necessary minority carriers. The resistive path from any point in the inverted layer to the diffusion layer should be kept to a minimum to minimize voltage drops and hence errors in the actual voltage applied across the dielectric. For PMOS/P-poly capacitors tested in inversion, there is also a voltage drop due to the depletion region in the p^+ gate electrode that must be considered.

The test capacitor should not have contacts or probe pads over the thin oxide region. Compressive stress caused by probing pads over oxides can result in device damage and inaccurate defect density measurements.

In order to determine the voltage acceleration parameter γ and the thermal activation energy required to extrapolate product lifetime from accelerated stress conditions, the CVS test is performed at several voltages and temperatures. Although log-normal statistics can be used to fit the failure distribution, Weibull statistics are recommended. The parameter γ is the slope of the $\ln(t_{63})$ vs. V_{stress} plot. t_{63} is the modal value of the Weibull distribution. To determine the thermal activation energy, it is necessary to perform the test at several temperatures. Stress voltages are selected to provide reasonable test times.

Note that the extrapolated product lifetime must also take into consideration the difference in area between the test devices and the product. It is recommended that at least three different test structure areas be used in characterizing the area dependence of time-dependent dielectric breakdown. One of the properties of Weibull statistics is a shift of the distribution with device area. Area scaling of time-to-breakdown, T_{BD} , can be defined as follows [1]:

$$\frac{T_{BD1}}{T_{BD2}} = \left[\frac{A_2}{A_1} \right]^{1/\beta}$$

4 Constant voltage test procedure (cont'd)

4.1 Test configuration

T_{BD1} is time-to-breakdown for device of area A_1 and T_{BD2} is time-to-breakdown for device of area A_2 . β is the Weibull shape factor. Observing the above area dependence will give confidence that the measured breakdown times are valid.

The sample size at each stress point should be carefully chosen to provide acceptable confidence limits. See JESD35, Annex C, for guidelines on acceptable sample size. Also confidence limits should be calculated for each data set. Please see [2] for calculating confidence bounds for Weibull distributions. To accurately model intrinsic oxide wear-out, the extrinsic failures may be censored. Large test sample size can be used to reveal the extrinsic or defect “tail”.

The following clauses describe the details of the constant voltage stress test. This measurement is performed in four parts. First, a pre-test checks for ‘initial’ failures. After this, a constant voltage is applied until oxide breakdown. Finally a post-test determines the final state of the oxide structure.

4.2 Pre-characterization test

A pre-characterization test obtains several baseline parameters required to successfully implement the CVS test. This test requires that the test equipment current compliance (I_{comp}) is at least 10 times greater than I_{stress} and that the value of I_{use} is greater than the test system noise.

In this test the following baseline parameters are determined from known “good” devices:

- a) Typical values of I_{stress} at all selected values of V_{stress} and I_{use} at V_{use} .
- b) Baseline values for system current noise at all selected values of V_{stress} .

The pre-characterization test should be performed on at least 5 samples distributed across the wafer. The CVS test V_{stress} values are selected to provide long enough breakdown times to provide adequate time resolution and short enough to provide reasonable test times.

A voltage ramp test is used to obtain typical values for I_{stress} at V_{stress} and I_{use} at V_{use} . The voltage ramp should be applied using the following parameters (See JESD35 for more details):

- Ramp Rate: 1 MV/cm-s
- Step Height: not to exceed 0.1 MV/cm
- Voltage Step Time: less than 0.1 s
- Current Measurement Interval: minimum once per step.
- Maximum Voltage: 30 MV/cm

4 Constant voltage test procedure (cont'd)

4.2 Pre-characterization test (cont'd)

Device breakdown is determined during the ramp by observing an abrupt increase in current. If no breakdown is evident, then a smaller device area could be used (see Annex A on test structures) or the increase in SILC can be used to detect breakdown as discussed in 4.4.3 (c). This method monitors the increase in SILC after each voltage step. Immediately after each voltage step the voltage is dropped to (V_{SILC}) and I_{SILC} is measured after a wait time (t_{wait}) to allow any transients to diminish such that I_{SILC} settles to a constant value. The value of V_{SILC} is typically 1 V to 2 V. Depending on the test system typical t_{wait} values could be several seconds.

See [3] for a description of a voltage ramp procedure using the I_{SILC} method. During the voltage ramp test record typical values and value range for I_{stress} at V_{stress} and I_{use} at V_{use} .

Baseline values for system current noise at V_{stress} is obtained by applying V_{stress} and calculating several values of the current noise as defined in 4.4 (b). These values should be obtained prior to device failure and an average of at least 5 values should be calculated.

4.3 Pre-CVS oxide current test

The purpose of the pre-test is to identify initial device failures. In addition, an optional leakage current (I_{leak}) test can be applied for specific studies.

- 1) Set and record stress temperature. Temperature should be controlled within ± 2 °C.
- 2) Determine typical I_{use} values at V_{use} as described in the pre-characterization test 3.2.
- 3) Force V_{use} .
- 4) Measure I_{meas} .
- 5) If $I_{meas} > 10 \times$ average value I_{use} determined from the pre-characterization test, record as initial failure.
- 6) Optional: If $I_{meas} > I_{leak}$, record as yield failure.

4 Constant voltage test procedure (cont'd)

4.4 Constant voltage stress test

Devices that pass the pre-CVS test are then subject to the constant voltage test. In order that the compliance circuit in the test equipment does not interfere with the determination of breakdown it is recommended that the compliance of the test system (I_{comp}) be at least 10X greater than I_{stress} [4].

- 1) Apply or ramp the voltage to the stress voltage (V_{stress}) ensuring that voltage overshoots do not exceed 1% of V_{stress} . The voltage ramp time should be less than 1% of the anticipated time-to-fail (t_{bd}). The minimum value is 100 ms.

After the voltage ramp, the voltage is held at V_{stress} and the current is periodically monitored and logged to a data file. The current can be monitored at short time intervals (t_{meas}); however, the current should be recorded in the data file at time intervals (t_{record}). The record time interval should be less than 1% of the anticipated time-to-fail (t_{bd}). For practical considerations t_{record} can be evenly spaced log time intervals. The logged data can be used to validate the actual breakdown event.

- 2) The device is considered to have failed when one of the following breakdown conditions has been detected:
 - a) Increase in measured oxide current

For thicker oxides ($t_{\text{ox}} > 5 \text{ nm}$) or for small area test structures the oxide often fails by a sudden increase ($>10\text{X}$) in measured oxide stress current.

$$I_{\text{meas}} > 10 \times I_{\text{previous}}$$

If this condition is met the test is terminated and the post-test is performed. Note that value of 10X increase is a recommended value. This value could range between 2-10X for actual hard breakdown events depending on capacitor area, thickness, structure, or process.

The breakdown time and I_{meas} should be recorded. The breakdown is classified as “Hard”.

4 Constant voltage test procedure (cont'd)

4.4 Constant voltage stress test (cont'd)

b) Increase in current noise [5]

At a soft-breakdown oxide event the measurement noise increases. This increase in noise can be detected by analyzing the current measurement data using variance techniques. This test description assumes that the test system noise has already been determined as described in the pre-characterization test (See 4.2).

In this test six consecutive current values of $I_{\text{meas}}(i)$ to $I_{\text{meas}}(i+5)$ are recorded and the current noise $(\delta I_{\text{meas}})^2$ is calculated from these values as:

$$(\delta I_{\text{meas}})^2 = \frac{\sum_{i=1}^{i=5} \{I_{\text{meas}}(i)\}^2 - \frac{\left[\sum_{i=1}^{i=5} I_{\text{meas}}(i) \right]^2}{5}}{4}$$

NOTE The final value of $(\delta I_{\text{meas}})^2$ is essentially the estimator of the sample variance of five I_{meas} values.

The current noise is continually calculated by adding a new current value and deleting the first value in the six-point set (i.e., a sliding sample set: $I_{\text{meas}}(i+1)$ to $I_{\text{meas}}(i+5)$). If the current noise increases by 500X over the baseline value determined in 3.2 for at least five additional calculations, then the device is defined as failed. The additional calculations performed past the detection of breakdown assures that the noise increase is sustained and not a result of a random fluctuation or a transient noise increase. The test is then terminated and the post-test performed. Note that value of 500X increase is a recommended value. This value could range between 200X and 500X for actual soft breakdown events depending on capacitor area, thickness, structure, or process.

It may be desirable to compensate for slowing increasing values of I_{meas} during the stress due to trapping or stress-induced leakage current. In this case, the value of $(\delta I_{\text{meas}})^2$ can be calculated from the variance of five values of the *difference* between the $I_{\text{meas}}(i+1) - I_{\text{meas}}(i)$ data points in the six point sample as follows:

$$(\delta I_{\text{meas}})^2 = \frac{\sum_{i=1}^{i=5} \{I_{\text{meas}}(i+1) - I_{\text{meas}}(i)\}^2 - \frac{\left[\sum_{i=1}^{i=5} I_{\text{meas}}(i+1) - I_{\text{meas}}(i) \right]^2}{5}}{4}$$

4 Constant voltage test procedure (cont'd)

4.4 Constant voltage stress test (cont'd)

Figure 1 illustrates a typical example of implementing the variance method for detecting breakdown. The example is for a 2.0 nm thick SiO₂ sample with an area of $4 \times 10^{-6} \text{ cm}^2$. Note that more than a four-order-of-magnitude increase in the current noise is observed at the onset of dielectric breakdown.

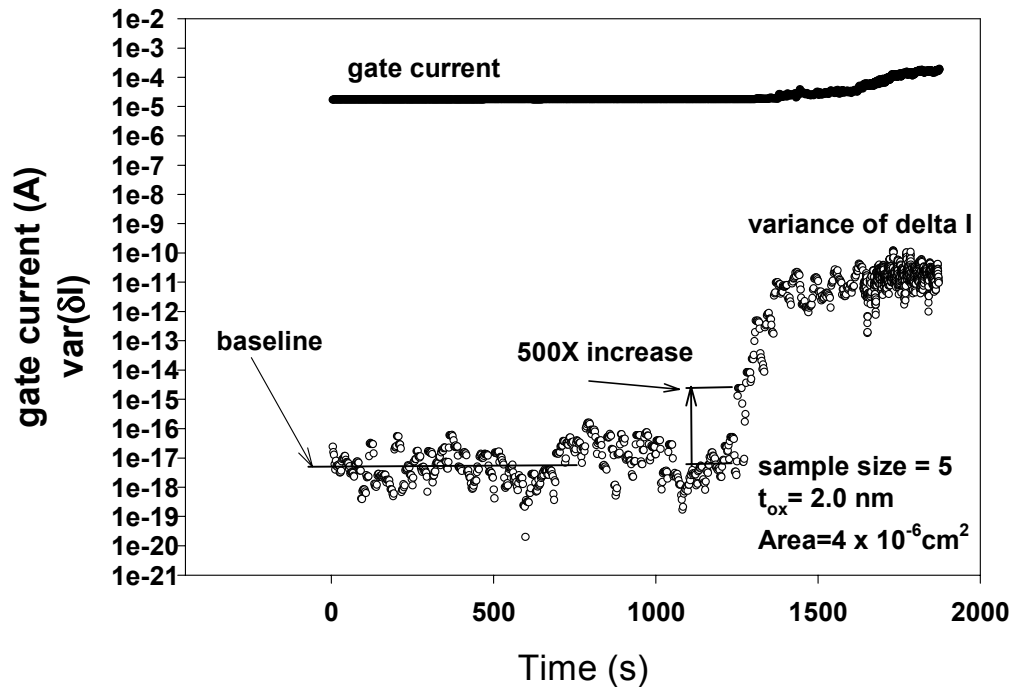


Figure 1 — Stress gate current vs. time and gate current noise vs. time for a 2.0 nm thick SiO₂ film with an area of $4 \times 10^{-6} \text{ cm}^2$. The onset of breakdown is detected by a >500X increase in the current noise.

Ultra-thin oxides have been observed to exhibit rapid current transients and random telegraph signals (RTS) before breakdown. Care must be taken to avoid detecting breakdown under these conditions. A technique described in [6] has been shown to reduce sensitivity to RTS and other transient behavior.

The breakdown time and pre/post breakdown noise level should be recorded. The breakdown is classified as “Soft”.

4 Constant voltage test procedure (cont'd)

4.4 Constant voltage stress test (cont'd)

c) Increase in low voltage stress-induced leakage current (SILC)

This method monitors the increase of SILC as a function of stress time to determine when soft-breakdown has occurred. In this technique at periodic time intervals (t_{int}) the voltage stress is interrupted and device current (I_{meas}) measured at low gate voltage (V_{SILC}). The value of V_{SILC} is typically 1 V to 2 V. After stress interruption and before the I_{meas} measurement a wait time (t_{wait}) should occur to allow any transients to diminish which may occur in some test systems. The t_{int} value should be $< 1\%$ of the anticipated t_{bd} while t_{wait} should be determined for each stress condition such that I_{SILC} settles to a constant value. Depending on the test system typical t_{wait} values could be several seconds. The I_{SILC} value should also be recorded to a data file.

If $I_{meas}(V_G, t_{int+1}) > F \times I_{meas}(V_G, t_{int})$, then the device is defined as failed. The test is terminated and the post-test is conducted. Typical values of F are between 2 to 5. The value depends on t_{ox} , A_{oxide} , and V_{SILC} .

Figure 2 shows block and timing diagrams describing the stress interruption technique. It has been shown that periodic stress interruption does not affect the lifetime distributions for a variety of stress conditions [7,8].

The breakdown time and pre/post breakdown I_{SILC} level should be recorded. The breakdown is classified as “Soft”.

4 Constant voltage test procedure (cont'd)

4.4 Constant voltage stress test (cont'd)

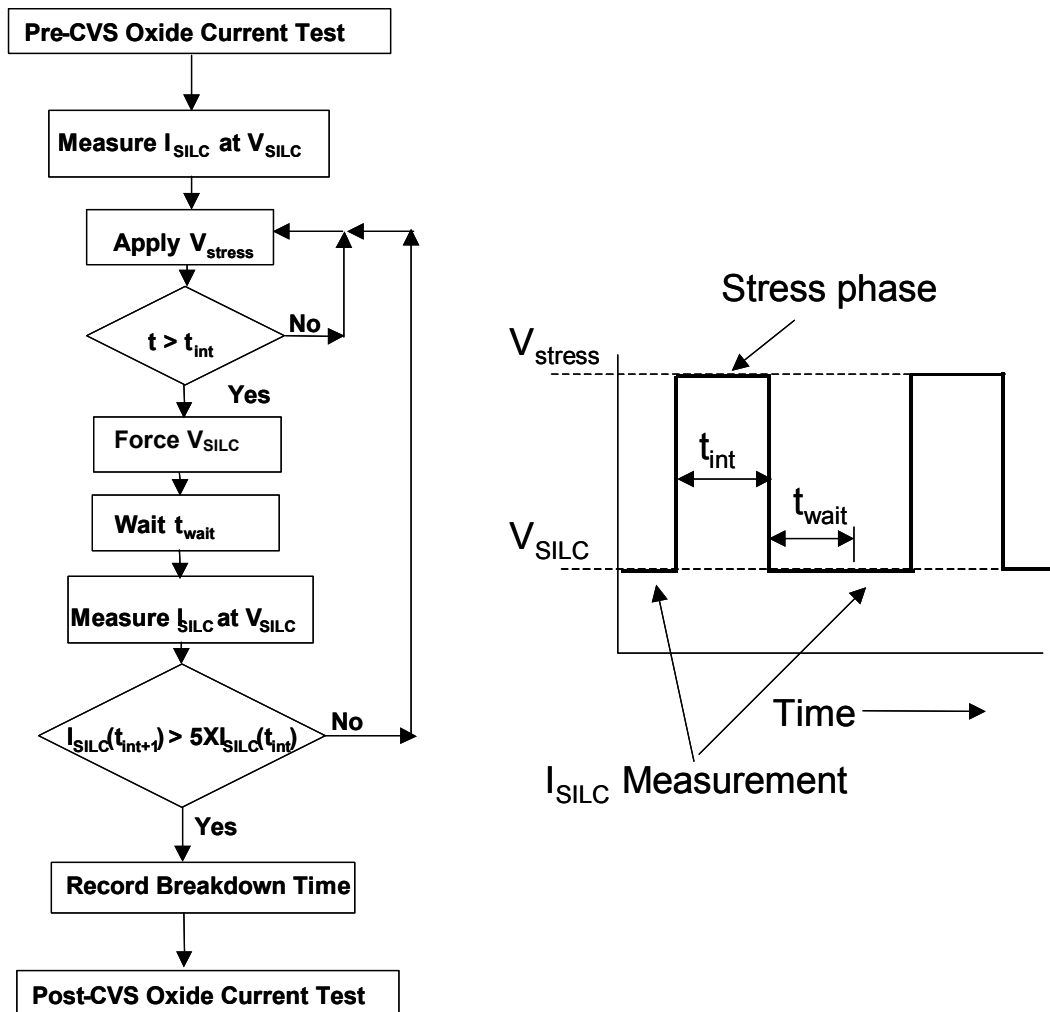


Figure 2 — Block diagram and timing diagram showing the implementation of the stress interruption technique for monitoring the change in SILC (t_{int} must be $< 1\%$ of the anticipated t_{bd}).

4 Constant voltage test procedure (cont'd)

4.5 Post-CVS oxide current test

Following breakdown detection as defined in 4.4 or if the test is user terminated, a post-test similar to the pre-test should be conducted as follows:

- 1) Force V_{use}
- 2) Measure I_{meas}
- 3) If $I_{meas} > 10 \times I_{use}$, record as Catastrophic Failure. (Note that this condition is expected to be false in all cases where soft breakdown occurred and was detected by the noise or SILC detection methods discussed in 4.4.)

4.6 Data recording

For all catastrophic failures (desired failure category, see Table 1) record the following information as outlined below.

- t_{bd} - oxide time-to-breakdown.
- q_{bd} - the accumulated oxide breakdown charge density.
- Failure category – the oxide failure mode as defined in 4.7.

In addition it is recommended that the following parameters be recorded:

- $I_{bd}(V_{stress})$ - the oxide breakdown current measured at the stress voltage.
- (Optional) $I_{bd}(V_{low})$ - the oxide breakdown current measured at a defined low voltage.

4 Constant voltage test procedure (cont'd)

4.7 Oxide failure categories

Because of the complexity of the oxide test procedure, five possible oxide failure types can occur. These failure types are listed in Table 1 and discussed in this section:

Table 1 — Oxide failure categories

| Stress failure type | Pre-test | CVS test | Post-test | Recorded parameters |
|---------------------|----------|----------|-----------|--|
| Type I | Fail | N/A | N/A | Failure type I |
| Type II.x | Pass | Fail | Fail | Failure type II, t_{bd} , I_{bd} (V_{stress}), $(\delta I_{meas})^2$ or I_{SILC} |
| Type III | Pass | Pass | Fail | Failure type III |
| Type IV.x | Pass | Fail | Pass | Failure type IV, t_{bd} , I_{bd} (V_{stress}), $(\delta I_{meas})^2$ or I_{SILC} |
| Type V | Pass | Pass | Pass | Failure type V |

NOTE The “x” indicates what breakdown criterion was used to detect breakdown: x = 1 (compliance or $I_{meas} > 10 \times I_{previous}$), x = 2 (current noise), x = 3 (change in I_{SILC}). Pass in the pre-test indicates that the initial oxide current did not exceed the failure criteria, i.e., the oxide was not “shorted”. Pass in the post-test also indicates that the oxide current did not exceed the failure criteria, i.e., it was not “shorted”. Pass in the CVS test indicates that oxide breakdown was not detected with one of the failure criteria specified in 4.4.1.

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Annex A (informative) Supplemental data analysis

A.1 Test structures

In order to minimize extrinsic defects and determine the intrinsic oxide breakdown behavior relatively small area test structure should be used. The failure time is a function of area, even in the absence of gross defects. In practical terms, capacitor areas in the range of 1k to 10k μm^2 are typically suitable for TDDB testing of ultra-thin oxides. It should be noted that the tunneling current for oxides less than 5 nm can become significant for large area test structures. Device breakdown will become very difficult to detect if the jump in leakage current associated with the breakdown event is of the same magnitude as the tunneling current. For oxides with t_{ox} less than 2 nm it may become necessary to limit the test structure area to less than 2.5k μm^2 depending on the magnitude of the tunneling current. Structures may be chosen to emphasize specific geometry, e.g., poly edge or field oxide isolation edge. Small area single transistors may also be used, but should have much longer failure times.

It is important to minimize the series resistance of the capacitor electrodes. Series resistance effects cause parasitic voltage drops reducing the effective voltage and electric field across the oxide.

Capacitors with large area polysilicon or metal electrodes (not necessarily large antenna ratios) are susceptible to plasma charging and damage. This should be considered in assessing TDDB data. Diode protection may be appropriate, although it restricts the applied stress voltage polarity and maximum voltage that can be used. Therefore, antenna structures should also be characterized to assess plasma charging.

A.1.1 Test structure design considerations

Three basic types of test capacitors are essential for oxide reliability characterization. These are area intensive, gate-edge intensive, and field-oxide-isolation-edge intensive capacitors. An array of MOSFETs can also be used. TDDB testing is commonly used to measure intrinsic oxide wearout. Wearout is often associated with area intensive capacitors. However it is important to recognize that product lifetime, even intrinsic wearout, may be dominated by the oxide reliability at the gate edge or at the edge of the thick thermal oxide. An area intensive capacitor is one with a large area component relative to edge components. A gate-edge capacitor is designed with maximum gate edge over thin oxide and has minimum area and field-oxide edge. Similarly, the field-oxide-isolation-edge capacitor maximizes the field oxide isolation edge component while minimizing the other two. With three capacitors and three different ratios of the three components it is possible to determine each failure density contribution to the overall oxide reliability.

Annex A (informative) Supplemental data analysis (cont'd)

A.1.2 Process plasma charging effects

Test structures with a variety of charge collection antennas are used to assess the effect of plasma charging damage on oxide reliability. The effect is related to the efficiency of charge collectors called antennas. Test structures often have large bond pads and a different ratio of contact to capacitor area than transistors in a product. Because of these differences the test capacitor may not be representative of product transistors. Therefore test capacitor evaluation using different antenna types and sizes is desirable.

The gate-electrode antenna ratio (charge collection efficiency) is defined as a ratio of the antenna area to the thin oxide area. It can also be defined in terms of the ratio of the antenna perimeter to the capacitor area. Either factor can be important depending on the processing conditions. Capacitors with antennas that have different area and edge components allow processing steps and their effect on oxide quality to be characterized. In addition, metal interconnect and via processing including the bond pad can cause oxide charging damage. Metal interconnect charging damage can be characterized by metal antennas with different interconnect areas and edge ratios. The via or contact process charging damage can be characterized by antennas with different number of contacts or vias. In this case the number of contacts or vias divided by the capacitor area is a measure of the charge collection efficiency.

A.1.3 Avoiding design pitfalls

Good test structure design must minimize several oxide-current-related effects. The test structure must be able to sustain high stress currents. The design must maintain a uniform electric field over the oxide area in spite of potential parasitic voltage drops in the substrate and the gate electrodes associated with the high stress current. The performance of the test structure must not degrade due to high-current-induced interconnect, contact, or via electromigration. Large peak currents may occur during the oxide rupture event causing metal open circuits or contact burn-out. Displacement currents occurring during the voltage must be differentiated from the actual stress current. Displacement currents are due to the charging of parasitic instrument cable and switching matrix capacitance as well as the test capacitor itself. The parasitic instrumentation capacitance can be greater than the actual test structure capacitance. Other effects to consider are parasitic surface leakage, metal bridging, conductive particles, or other defects.

Annex A (informative) Supplemental data analysis (cont'd)

A.1.3.1 High stress currents

The test structures should be designed to keep the electric field uniform over the capacitor area. One way to accomplish this is to use rectangular test structures. The gate electrode should have multiple contacts along one of the long edges, (no polysilicon contacts should be placed over thin oxide). Substrate contacts should be placed along the long edge opposite the gate contacts. Due to high stress currents there will be voltage drops in the gate electrode and substrate. By placing the contacts along opposite sides of the capacitor the voltage drops will compensate one another keeping the electric field as uniform as possible over the capacitor area. The typical aspect ratio of rectangular capacitors is 1:5 to 1:10. The greater the sheet resistance difference between the gate and substrate, the larger the aspect ratio should be.

To avoid high stress current and possible electromigration, use wide metal and polysilicon interconnects. The number of contacts and vias should be sufficient to avoid contact electromigration. Although the maximum number and thickness of conductor lines is desirable for minimal resistive drops, the area above the capacitors should be kept as clear as possible to facilitate failure analysis.

The test structure total series resistance should be as low as possible. Series resistance effects cause parasitic voltage drops leading to reduced stress voltages and currents and longer TDDb lifetime than expected.

A.1.3.2 High currents during oxide breakdown

During the breakdown event, extremely high transient currents flow. Initially the discharge current comes from the charge stored on the test capacitor. The peak current is limited by the current dynamics in the breakdown plasma and the resistance of the gate and substrate electrodes. The greater the local oxide voltage the greater the energy released into the breakdown event. Test structure design has little effect on this part of the discharge event if the capacitor plate is a single sheet or has been designed to take this large current level into account. If the capacitor is an array of many small capacitors, the whole array charge is conducted through the gate connection to the capacitor that ruptured. If the capacitor gate connection is narrow or has few contacts, the connection may open and the breakdown event may go undetected.

The greater the capacitance voltage the greater the energy provided by the instrumentation cables and supplies for the breakdown event. When the capacitor's voltage suddenly drops, the instrumentation cables behave as a transmission line. Extremely high peak current occurs, limited mainly by the cable's inductance and characteristic dynamic impedance. The series resistance of the test structure may also limit the current, but since the series resistance should be so low high current can flow. This high current flows through the interconnect and can cause via and contact open circuit damage. Increasing interconnect width and number of vias and contacts should prevent this damage from occurring.

Annex A (informative) Supplemental data analysis (cont'd)

A.1.3.3 Displacement currents

Test structure and the test instrumentation charging characteristics should be measured. It is important that the instrumentation settling time be much less than the time to failure. Minimizing the instrumentation cable capacitance makes it easier to detect oxide breakdown events and minimize the effect of cable capacitance discharge effects on the breakdown damage. Large instrumentation capacitance may cause the breakdown event to go from a soft to a hard failure.

A.1.3.4 Parasitic leakage

At the completion of the test, failure analysis should be performed on representative capacitors. This is done to ensure that failure statistics include only valid oxide failures and that no breakdown events go undetected due to a faulty test structure design. A visual inspection should be made to verify that the breakdown locations occurred at random locations over the test structure area. The failure location should not show a systematic pattern such as failing at a corner or near an interconnect lead.

The test capacitor may include an isolating guard ring, especially when testing several devices in parallel. This guard ring encircles the test capacitor and can be used to detect and minimize lateral test structure leakage paths.

A.1.3.5 Miscellaneous test issues

If lifetime tests are being performed at high temperature, the sheet resistance increases. This increased sheet resistance may affect the electric field uniformity across the capacitance area and the test structure series resistance.

Scribe-line test structures may receive slightly different processing conditions compared to oxides within the circuit. This may lead to TDDB test result differences.

If the entire wafer is dedicated to oxide test capacitors, micro-loading effects might change the processing conditions. Cross section checks should be made to confirm that field-oxide-edge profile, poly gate side-wall construction, and other critical dimensions still represent those of product transistors.

Metal gate capacitors are prone to self-healing. Self-healing occurs when the metal vaporizes above the rupture site creating an open rather than an oxide short. Breakdown events of this type may go undetected.

Substrate voltage drops can alter the stress conditions of nearby capacitors when testing devices in parallel. Separate wells and well contacts are recommended for each device. Adding substrate guard rings can help control the substrate potential. The substrate potential needs to be considered at normal stress conditions and after capacitor breakdown.

Annex A (informative) Supplemental data analysis (cont'd)

A.1.3.6 Test Structure verification

Each test capacitor's current (Log(I)) vs. voltage characteristic should be compared to theory. Deviations from theory may be due to series resistance effects. These measurements should be performed at both room and the stress temperature.

SEM cross sections should be made on each test structure to validate critical dimensions.

A.2 Determining oxide electric field

As device dimensions are reduced into the deep submicron regime, oxide thickness, oxide voltage, and parasitic voltage drops in the polysilicon gate and substrate must be considered if accurate TDDB measurements are to be made. The discussion below is divided into two sections depending on the thickness of the oxide.

$$t_{ox} > 5 \text{ nm}$$

An accurate determination of oxide field is essential if the underlying physical mechanism for dielectric breakdown is to be understood.

The electric field across the capacitor (E_{ox}) is given by:

$$E_{ox} = \frac{V_{ox}}{T_{ox}} \quad (1)$$

where

$$V_{ox} = V_g - V_{FB} - V_s - V_p \quad (2)$$

and V_g is the applied gate voltage, V_{FB} the flat-band voltage, V_s the surface potential of the well, and V_p the voltage drop in the polysilicon (polysilicon depletion term) which is negligible in accumulation only for dual work-function technologies and not for single work-function technologies.

Annex A (informative) Supplemental data analysis (cont'd)

A.2 Determining oxide electric field (cont'd)

For oxide thickness above 4 nm, the oxide field can be extracted from the Fowler-Nordheim tunneling current and is given by:

$$J_{FN} = AE_{ox}^2 \exp\left(-\frac{C}{E_{ox}}\right) \quad (3)$$

where A and C are constants and given by:

$$A = \frac{q^3}{8\pi\pi} \left(\frac{1}{\Phi_B m^*} \right) \quad (4)$$

and

$$C = \frac{8\pi\sqrt{2}}{3qh} \left(\frac{m^*}{m} \right)^{1/2} \Phi_B^{3/2} \quad (5)$$

where m^* is the electron effective mass (~ 0.5). Φ_B is the oxide barrier height (~ 3.1 eV).

$$t_{ox} < 5 \text{ nm}$$

For ultra-thin oxides (with $t_{ox} < 5$ nm) the gate voltage is more important to quantify than the oxide electric field. In this case, quantum-mechanical and polysilicon depletion effects can have a significant impact on determining the actual voltage applied between the anode and the cathode of the dielectric. In this case special CV analysis tools have to be used to determine the effective oxide voltage and thickness. Please see [9] for a description and a comparison of the various simulation codes available.

A.3 Extrapolation models

The discussion below is divided into two sections depending on the thickness of the oxide.

$$t_{ox} > 5 \text{ nm}$$

Two field dependent lifetime (E_{ox} and the $1/E_{ox}$) models are commonly used to analyze oxide breakdown data. The E_{ox} model is based on a thermochemical model [10,11] for oxide breakdown. In this model oxide breakdown is due to coupling between the applied electric field (E_{ox}) with the oxide dipole moments (field enhanced bond breakage) and predicts that the time to breakdown (T_{bd}) has an exponential linear dependence on applied electric field

$$T_{bd} = \tau_0(T) e^{-\gamma(T) E_{ox}} \quad (1)$$

where τ_0 and the field acceleration factor (γ) are temperature (T) dependent fit parameters. Parameter values of $\tau_0 = 1.0 \times 10^{-11}$ s and $\gamma = 2.66$ cm/MV fit a wide oxide thickness range (11.0 nm – 22.5 nm) and oxide technologies [12].

Annex A (informative) Supplemental data analysis (cont'd)

A.3 Extrapolation models (cont'd)

The $1/E_{ox}$ model is based on the anode hole injection model [13,14]. In this model accelerated Fowler Nordheim (FN) injected electrons (Note: $I_{FN} \sim e^{-B/E_{ox}}$) generate holes at the anode. These holes are back-injected and trapped in the oxide. Trapped holes increase the localized electric field resulting in increased tunneling current and a positive feedback mechanism leading to oxide breakdown. In the $1/E_{ox}$ model the T_{bd} has an exponential linear -+dependence on inverse electric field ($1/E_{ox}$)

$$T_{bd} = \tau_1(T) e^{-G(T)/E_{ox}} \quad (2)$$

where τ_1 and G are temperature (T) dependent fit parameters. For this model parameter values of $\tau_1 = 1 \times 10^{11}$ s and $G = 350$ MV/cm fit a wide oxide thickness range (5.2 nm to 17.0 nm) and oxide technologies [12].

Considerable controversy exists between which model correctly describes oxide breakdown phenomenon. This controversy occurs because both E_{ox} and $1/E_{ox}$ models fit high field breakdown data (> 10 MV/cm) equally well but differ by orders of magnitude in their lifetime prediction at use bias condition. Experimental findings [15, 16] suggest that the E_{ox} model is the better fit to low electric field data and therefore recommended for lifetime prediction.

A unified oxide breakdown model has recently been proposed [17, 18] that combines the E_{ox} and $1/E_{ox}$ models. The assumption here is that both enhanced bond breakage and hole generation and trapping processes coexist contributing to oxide degradation. This model proposes that T_{bd} can be expressed as:

$$1/T_{bd} = 1/T_{bd1} + 1/T_{bd2} \quad (3)$$

where T_{bd1} and T_{bd2} are the lifetimes predicted by the E_{ox} and $1/E_{ox}$ respectively. Physically, this model predicts that at low electric fields where FN current is small the E_{ox} model dominates while at high electric fields where FN current is large the $1/E_{ox}$ model dominates.

$$t_{ox} < 5 \text{ nm}$$

It should be mentioned that recent analysis of breakdown data suggests that the breakdown mechanism is a voltage-driven process as oxide thickness is decreased. It is therefore appropriate to analyze the breakdown data in terms of V_{ox} not E_{ox} . Wu, et al. examined very large TDDB data sets of ultra-thin oxides and demonstrated that t_{BD} had the functional form of $t_{BD} \sim V^{-n}$ where n was independent of thickness [19]. This model should be considered equally with the V_{ox} and $1/V_{ox}$ models described above.

Annex A (informative) Supplemental data analysis (cont'd)

A.4 Determining failure rates

- FIT calculation:

Given that a device under test survives up until time t , the instantaneous failure rate at time t is given by hazard function $h(t)$ as

$$h(t) = \frac{f(t)}{1 - F(t)}$$

where $f(t)$ is the probability density function (PDF) and $F(t)$ is the cumulative distribution function (CDF) or unreliability function.

The average failure rate of survivors over the time interval t_1 to t_2 is the integration of the hazard function $h(t)$, i.e.,

$$AFR(t_1, t_2) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} h(t') dt' = \frac{-\ln(1 - F(t_2)) + \ln(1 - F(t_1))}{t_2 - t_1}$$

and therefore the average failure rate (AFR) of survivors from time 0 to t is

$$AFR(t) = \frac{1}{t} \int_0^t h(t') dt' = \frac{-\ln(1 - F(t))}{t}.$$

The normal unit of AFR is the inverse of time, such as h^{-1} . 1 FIT is defined as 10^{-9} AFR.

Probability plotting (Weibull recommended) of time-to-breakdown t_{BD} gives distribution parameters needed to calculate the AFR. It is recommended that Weibull statistics be used in the case of ultra-thin oxides since it has been shown experimentally that it correctly predicts area scaling and the thickness dependence on Weibull slope. The distribution parameters are the scale parameter α and shape parameter β for the Weibull distribution. Table A.1 shows the equations for AFR calculation for the Weibull distribution.

Once the distribution parameters are known from the probability plotting, AFR can be calculated based on the equations in Table A.1. An easy way to do this is to use plotting paper or spreadsheet software that provides the built-in PDF $f(t)$, CDF $F(t)$ functions for both Lognormal and Weibull distributions.

Annex A (informative) Supplemental data analysis (cont'd)

A.4 Determining failure rates (cont'd)

Area scaling is another factor for AFR calculation. Assuming the defect distribution is random across the area (could also be randomly distributed across the field oxide edge), the reliability function $R(t)$ is

$$R(t) = 1 - F(t) = e^{-D_A A}$$

where A is the device area and D_A is the defect density.

For area A_1 and A_2 , we have

$$(1 - F(t)_{A_1})^{1/A_1} = (1 - F(t)_{A_2})^{1/A_2}$$

and therefore,

$$AFR_{A_1} = \frac{-\ln(1 - F(t)_{A_1})}{t} = \frac{-\ln(1 - F(t)_{A_2})}{t} \frac{A_1}{A_2} = AFR_{A_2} \frac{A_1}{A_2}.$$

A similar analysis can be performed for the defect density associated with edge or perimeter defects:

$$R(t) = 1 - F(t) = e^{-D_L L}$$

where L is the length of the device perimeter and D_L is defect density.

Table A.1 — Reliability characteristics for Weibull distributions

| Distribution parameters | Weibull |
|------------------------------------|--|
| PDF, $f(t)$ | $\frac{\beta t^{\beta-1}}{\alpha^\beta} \exp\left[-\left(\frac{t}{\alpha}\right)^\beta\right]$ |
| Unreliability, $F(t)$ | $1 - \exp\left[-\left(\frac{t}{\alpha}\right)^\beta\right]$ |
| Instantaneous failure rate, $h(t)$ | $\frac{\beta}{\alpha} \left(\frac{t}{\alpha}\right)^{\beta-1}$ |
| AFR | $\frac{1}{t} \left(\frac{t}{\alpha}\right)^\beta$ |

For additional information please see [20, 21].



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